ABSTRACT OF THE DISCLOSURE

The present invention relates to: a memory cell array which is capable of decreasing the parasitic capacitance of signal electrodes and has ferroelectric layers making up ferroelectric capacitors and having a predetermined pattern; a method of fabricating the memory cell array, and a ferroelectric memory device. In the memory cell array, memory cells formed of ferroelectric capacitors are arranged in a matrix. The ferroelectric capacitors include first signal electrodes, second signal electrodes arranged in a direction intersecting the first signal electrodes, and ferroelectric layers disposed linearly along either the first signal electrodes or the second signal electrodes. Alternatively, the ferroelectric layers may be disposed only in intersection areas of the first and second signal electrodes.